Lab 1: Logic Gates

**ITI 1100 C - Digital Systems**

**Fall 2016  
School of Electrical Engineering and Computer Science University of Ottawa**

Course Coordinator: Dr. Ahmed Karmouch

Teaching Assistants:

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TA 2 Name

Group 6

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Experiment Date: February 2, 2016

Submission Date: February 23, 2016

**Objectives**

* Construct simple combinational logic circuits from a schematic.
* Experimentally determine the functional operation of simple combinational logic circuits.
* Identify equivalent logic gates to those produced by various circuit configurations from the resulting truth table.
* Connect various gates together to create simple logic functions.
* Analyze combinational logic circuits and predict their operation.
* Construct and test more complex combinational logic circuits.

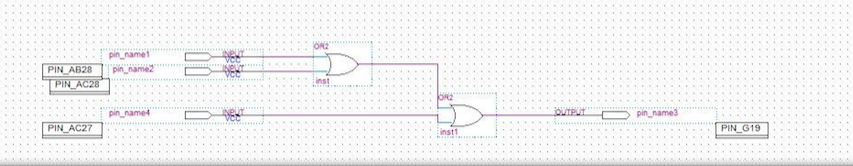
**Equipment & Components**

* Quartus II 13.0 Service-Pack 1
* Altera DE2-115 card

**Circuit Diagrams**

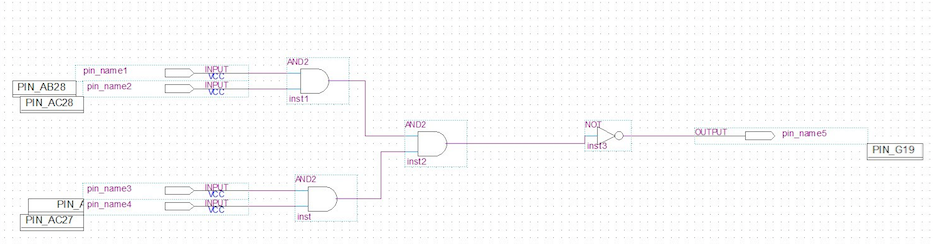
**Part I – Combinational Logic Circuit Construction**

***One-Chip Logic Circuit***



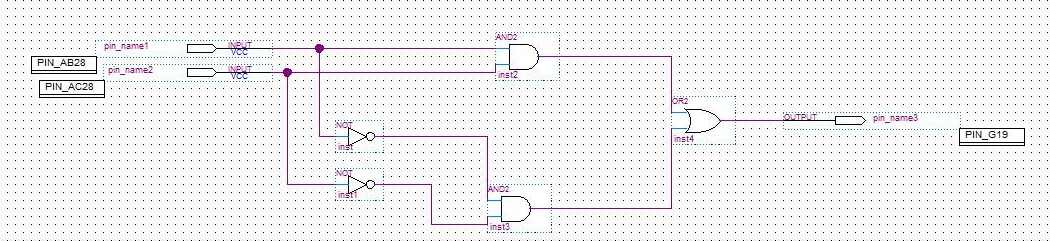
* **Figure 1: Screen-shot of One-chip logic circuit diagram  (Figure 5.1.1)**

***Two-Chip Logic Circuit***

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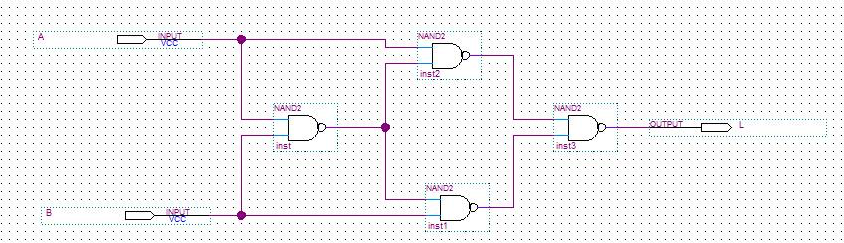
* **Figure 2: Screen-shot of Two-chip logic circuit diagram  (Figure 5.1.2)**

***Three-Chip Logic Circuit***



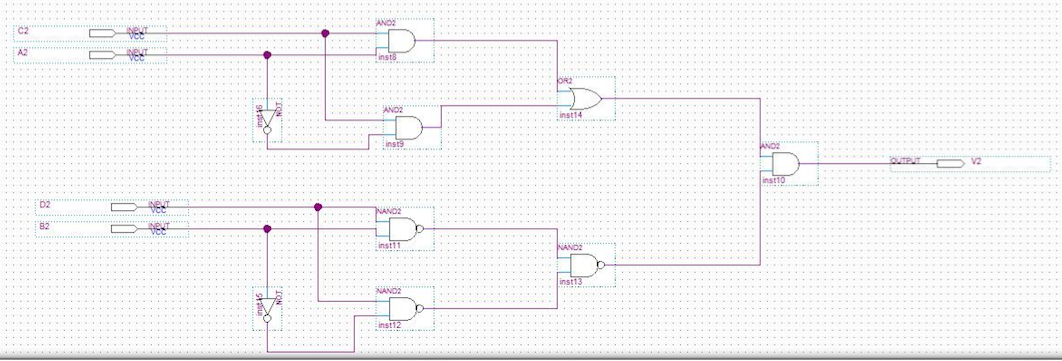
**Figure 3: Screen-shot of Three-chip logic circuit diagram  (Figure 5.1.3)**

* **Part II - Combinational Logic Circuits Analysis**

***Exclusive OR Circuit***

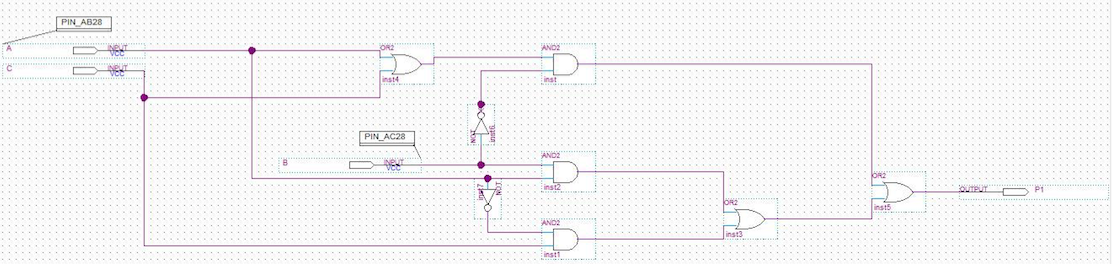
**Figure 4: Screen-shot of Exclusive OR logic circuit diagram  (Figure 5.1.5 of Lab Manual)**

***AND Circuit***



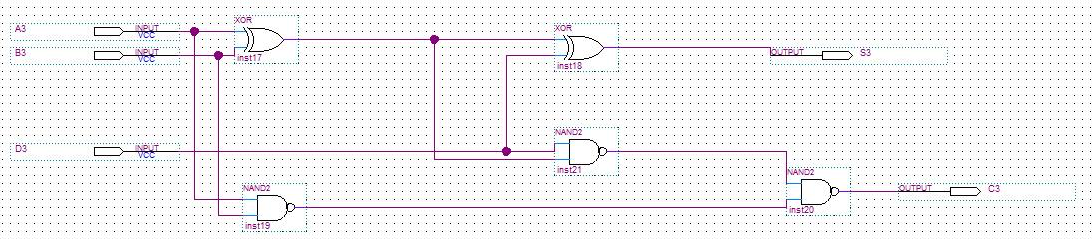
**Figure 5: Screen-shot of AND logic circuit diagram  (Figure 5.1.6 of Lab Manual)**

***OR Circuit***



**Figure 6: Screen-shot of OR logic circuit diagram  (Figure 5.1.7 of Lab Manual)**

***Multiple Output Circuit***

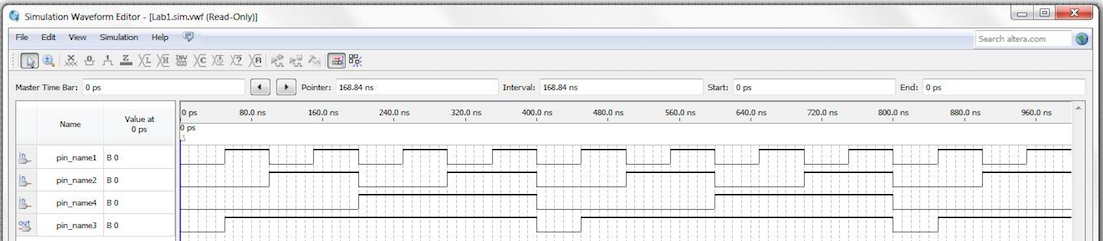


**Figure 7: Screen-shot of Multiple Output logic circuit diagram  (Figure 5.1.8 of Lab Manual)**

**Experimental Data and Data Processing**

**Part I – Combinational Logic Circuit Construction**

***One-Chip Logic Circuit***

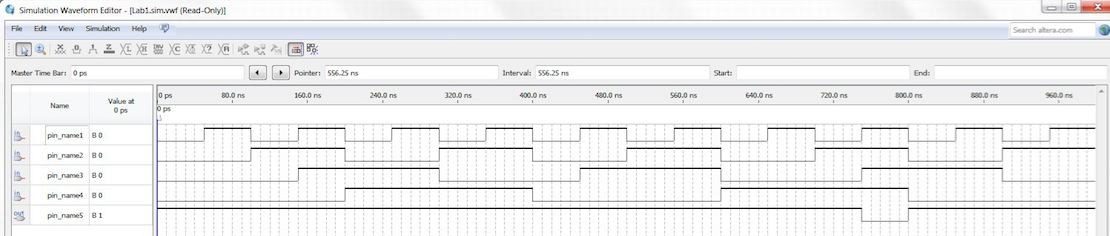


* **Figure 8: Simulation output waveform of one-chip circuit**

**Table 1: Experimental data observed from MAX 7000 Circuit Board**

|  |  |  |  |
| --- | --- | --- | --- |
| Input Given From Dip Switches | | | Observed Output from LED’s |
| **A** | **B** | **C** | **Output** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** |
| **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **1** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** |

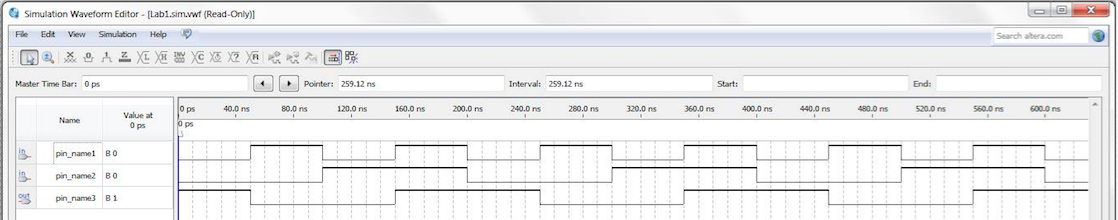
***Two-Chip Logic Circuit***



* **Figure 9: Simulation output waveform of two-chip circuit**
* **Table 2: Experimental data observed from MAX 7000 Circuit Board**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input Given From Dip Switches | | | | Observed Output from LED’s |
| **A** | **B** | **C** | **D** | **Output** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

***Three-Chip Logic Circuit***

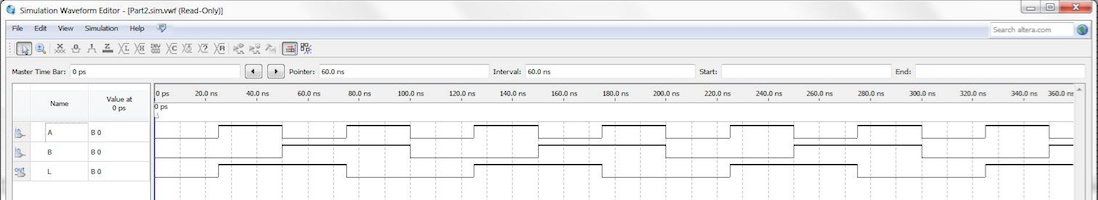


* **Figure 10: Simulation output waveform of three-chip circuit**
* **Table 3: Experimental data observed from MAX 7000 Circuit Board**

|  |  |  |
| --- | --- | --- |
| Input Given From Dip Switches | | Observed Output from LED’s |
| **A** | **B** | **Output** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

* **Part II - Combinational Logic Circuits Analysis**

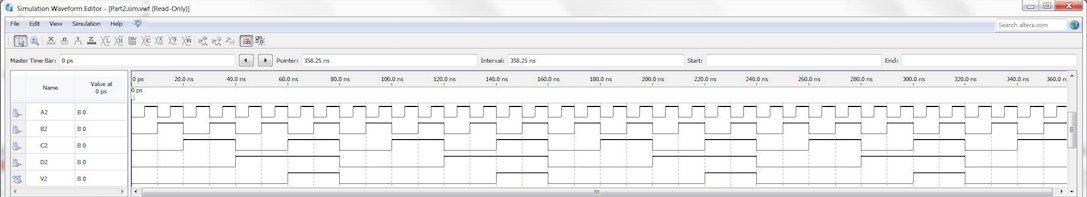
***Exclusive OR Circuit***



* **Figure 11: Simulation output waveform of exclusive OR circuit**
* **Table 4: Experimental data observed from MAX 7000 Circuit Board**

|  |  |  |
| --- | --- | --- |
| Input Given From Dip Switches | | Observed Output from LED’s |
| **A** | **B** | **L** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

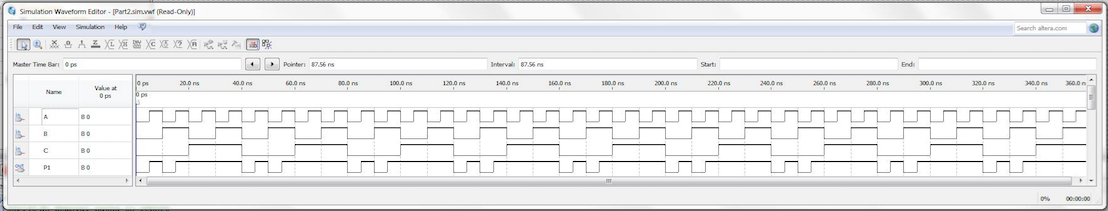
***AND Circuit***



* **Figure 12: Simulation output waveform of AND circuit**
* **Table 5: Experimental data observed from MAX 7000 Circuit Board**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input Given From Dip Switches | | | | Observed Output from LED’s |
| **A2** | **B2** | **C2** | **D2** | **V2** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

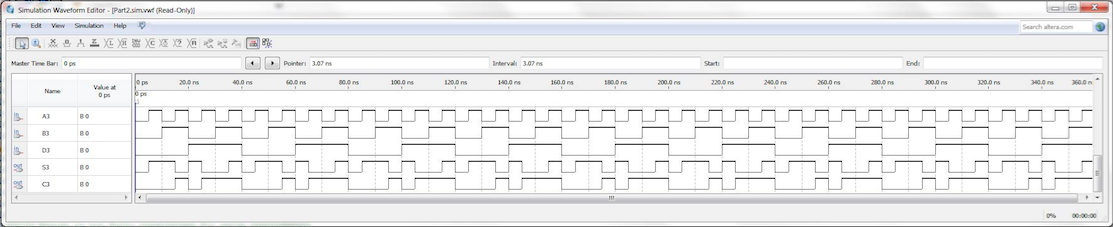
***OR Circuit***



* **Figure 13: Simulation output waveform of OR circuit**
* **Table 6: Experimental data observed from MAX 7000 Circuit Board**

|  |  |  |  |
| --- | --- | --- | --- |
| Input Given From Dip Switches | | | Observed Output from LED’s |
| **A** | **B** | **C** | **P1** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** |
| **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **1** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** |

***Multiple Output Circuit***



* **Figure 14: Simulation output waveform of Multiple Output Circuit**
* **Table 7: Experimental data observed from MAX 7000 Circuit Board**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input Given From Dip Switches | | | Observed Output from LED’s | |
| **A3** | **B3** | **D3** | **S3** | **C3** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Comparison of Theoretical Data and Experimental Data**

**Part I – Combinational Logic Circuit Construction**

***One-Chip Logic Circuit***

* **Table 8: Comparison of Theoretical and Experimental results for one-chip logic circuit**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | | **Expected Results** | **Actual Results** |
| **A** | **B** | **C** | **Output** | **Output** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The results observed experimentally for one chip circuit from MAX 7000 FGPA were identical to results obtained theoretically as expected.

***Two-Chip Logic Circuit***

* **Table 9: Comparison of Theoretical and Experimental results for two-chip logic circuit**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Expected Results** | **Actual Results** |
| **A** | **B** | **C** | **D** | **Output** | **Output** |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

The results observed experimentally for one chip circuit from MAX 7000 FGPA were identical to results obtained theoretically as expected.

***Three-Chip Logic Circuit***

* **Table 10: Comparison of Theoretical and Experimental results for three-chip logic circuit**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | **Expected Results** | | **Actual Results** |
| **A** | **B** | **OUTPUT** | **OUTPUT** | |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | |
| 1 | 0 | 0 | 0 | |
| 1 | 1 | 1 | 1 | |

The results observed experimentally for one chip circuit from MAX 7000 FGPA were identical to results obtained theoretically as expected.

* **Part II - Combinational Logic Circuits Analysis**

***Exclusive OR Logic Circuit***

* **Table 11: Comparison of Theoretical and Experimental results for exclusive OR logic circuit**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | **Expected Results** | | **Actual Results** |
| **A** | **B** | **L** | **L** | |
| 0 | 0 | 0 | 0 | |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 0 | |

The results observed experimentally for one chip circuit from MAX 7000 FGPA were identical to results obtained theoretically as expected.

***AND Logic Circuit***

* **Table 12: Comparison of Theoretical and Experimental results for AND logic circuit**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Expected Results** | **Actual Results** |
| **A2** | **B2** | **C2** | **D2** | **V2** | **V2** |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

The results observed experimentally for one chip circuit from MAX 7000 FGPA were identical to results obtained theoretically as expected.

***OR Logic Circuit***

* **Table 13: Comparison of Theoretical and Experimental results for OR logic circuit**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | | **Expected Results** | **Actual Results** |
| **A** | **B** | **C** | **P1** | **P1** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The results observed experimentally for one chip circuit from MAX 7000 FGPA were identical to results obtained theoretically as expected.

***Multiple Output Circuit***

* **Table 14: Comparison of Theoretical and Experimental results for Multiple Output logic circuit**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | **Expected Results** | | **Actual Results** | |
| **A3** | **B3** | **D3** | **S3** | **S3** | **C3** | **C3** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The results observed experimentally for one chip circuit from MAX 7000 FGPA were identical to results obtained theoretically as expected.